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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/065,503	10/25/2002	William R. Corbin	BUR920010217US1	2123

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IBM MICROELECTRONICS
INTELLECTUAL PROPERTY LAW
1000 RIVER STREET
972 E
ESSEX JUNCTION, VT 05452

EXAMINER	
KERVEROS, JAMES C	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 01/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/065,503	CORBIN ET AL.	
	Examiner	Art Unit	
	JAMES C KERVEROS	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 October 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☒ Claim(s) *1-11* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 December 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to Amendment filed October 14, 2004, responsive to the Office Action mailed June 14, 2004. Claims 1-14 are pending and presently under examination.

Claim objections, regarding the term "by pass" recited in claim 1, is withdrawn in response to the corrections in the Amendment.

Claim Rejections, for Claims 1-14 rejected under 35 U.S.C. 112, second paragraph, in reference to term " whereby", and for omitting essential structural cooperative relationships of elements, is withdrawn in response to the corrections made by the Amendment.

Drawings

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the "isolation elements" must be shown or the feature(s) canceled from the claim(s). No new matter should be entered. Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.121(d)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

The specification is objected to under 37 CFR 1.71 because it lacks an enabling description for claims 1-14, in reference to limitation "isolation elements" for logic and memory circuits, recited in the independent claims 1 and 12. The specification fails to point out the "isolation elements" in the disclosure.

Claim Objections

Claims 1-11 are objected to because of the following informalities:

Claim 1, as amended, recites the limitations "scan chain isolation elements; to enable and disable the BIST which tests the memory macro circuits while the logic scan chain results are read out". The limitations should be combined as follows: "scan chain isolation elements to enable and disable the BIST, which tests the memory macro circuits while the logic scan chain results are read out". Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 1-14 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art

to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

The specification fails to describe the claimed limitation "isolation elements" for logic and memory circuits, recited in the independent claims 1 and 12.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-14 are rejected under 35 U.S.C. 103(a) as being unpatentable Kraus et al. (US 6587979).

Regarding independent Claims 1, 12 and 14, Kraus substantially discloses an apparatus and method (FIG. 5) for performing parallel tests for logic circuits (14, 16) and for random access memories (RAM) 12 embedded an integrated circuit (IC) 10 with BIST circuit 11, comprising:

A clocking system (CLOCK) signal from IC tester (21, FIG. 5), which drives a sequencer 72 for producing the data pattern to be placed on the data input lines (DI) of RAM 12 (see FIG. 6)

In view of the claims rejected under 35 U.S.C. 112, first paragraph, for examination purpose, the Examiner broadly interprets the "isolation elements" to be equivalent to a core wrapper 24 positioned near each RAM 12 for isolating logic (14, 16) from the memory circuits (RAM) 12, where the wrapper includes scan chain bypass isolation elements (scan register 46) which enables and disables BIST 11, where the testing of the memory macro circuits (RAM) 12 is performed while the logic scan chain results are read out via a SCANOUT bus 23 to tester 21 by serially shifting the data outward from the logic circuits (14, 16).

Furthermore, Kraus discloses the step of verifying scan chain and BIST operation by loading BIST patterns from pattern generator (50, FIG. 6) clocked by the global (CLOCK) signal for writing and reading the data to / from RAM 12.

Kraus does not explicitly disclose voltage isolation elements for logic and memory circuits.

However, Kraus discloses scan register (46) within each core wrapper 24 connected to lines of the RAM bus 32 that convey the data output of RAM 12 to logic circuits (14, 16). During testing of logic circuits (14 and 16), IC tester 21 asserts a "scan force" mode in which the BIST circuit receives and stores data from the controller in the scan register and forces it onto the bus of an embedded RAM in response to a FORCE signal from the controller. This action allows tester 21 to bypass RAM 12, thus isolating the RAM memory from the logic without having to access data read out of the RAM 12.

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to use the force bypass testing signal, as taught by Kraus,

since the modified device of Kraus does not require additional voltage levels for isolating the logic and memory circuits. Thus testing RAM embedded in an IC allows a designer to flexibility to apportion test functions between internal BIST circuits and external test circuits and which can test embedded RAM of varying numbers and sizes in any of several ways, but which the designer can easily implement using standard cells requiring minimal modification (Col. 2, lines 32-40).

Regarding Claims 2-6 and 13, Kraus discloses bypass isolation elements (scan register 46) initiated by a control signal (FORCE) signal from the controller including testing the scan register 46 using Scan Force Mode. The FORCE signal line provides control of the multiplexer (48, FIG. 6), which connects the data out (DO) output port of RAM 12 to both test circuit 40 and to data out lines (DATA_OUT) of bus 32 leading to logic circuits 14 and 16 of FIG. 5.

Regarding Claims 7 and 8, Kraus discloses a control FORCE signal, which places the apparatus into bypass mode during the Scan Force Mode in which the BIST circuit receives and stores data from the controller in the scan register in response to the FORCE signal from the controller. After the BIST is completed the apparatus is taken out of bypass mode and into the "scan capture" mode in which the BIST circuit captures data appearing on each RAM's bus in a scan register in response to the CAPTURE signal from the external control and serially shifts it out to the controller in response to a SHIFT signal from the controller, described in the summary of the invention.

Regarding Claims 9,10 and 11, Kraus discloses a memory test clock (CLOCK signal) supplied by an external tester such as IC tester (21) to a control circuit located on the semiconductor device (IC) 10, which allows a logic test pattern from the pattern generator (50, FIG. 6) clocked by the (CLOCK) signal for writing and reading the data to / from RAM 12.

Response to Arguments

Applicant's arguments filed October 14, 2004 have been fully considered but they are not persuasive. Claims 1-14 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. Claims 1-14 are rejected under 35 U.S.C. 103(a) as being unpatentable Kraus et al. (US 6587979), as set forth in the present Office Action.

In reference to Claims 1-14 rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement, in regard to the limitation "isolation elements", recited in the independent claims 1 and 12, the Applicant indicated in his arguments that the specification provides explanation in paragraphs 24-27. However, the specification does not define or point out the "isolation elements". Instead, the specification points out to a clock arrangement, which is not related to the "isolation elements", where the "arrangement would provide sufficient isolation of the clock signals to be applied to the chip under test".

In reference to Claims 1-14 rejected under 35 U.S.C. 103(a) as being unpatentable Kraus et al. (US 6587979), the Applicant argues that Kraus discloses nothing about the parallel test of logic and memory. In response to Applicant's

argument, clearly Kraus performs testing for both logic circuits (14, 16) and for the random access memories (RAM) 12 embedded an integrated circuit (IC) 10 with BIST circuit 11, Figure 5. Kraus describes related to Figure 5, as follows, "a conventional external integrated tester 21 is provided to perform a logic test on logic circuits 14, 16 by applying input signal patterns to I/O terminals 18 and monitoring output signals patterns logic circuits 14, 16 produce at I/O terminals 18 in response to the input signal patterns". Furthermore, Kraus describes, "test system 17 includes a built-in self-test (BIST) circuit 11 incorporated into IC 10 for carrying out or facilitating any of several different types of tests on IC 10 including directly testing each RAM 12".

In response to Applicant's argument in reference to the interpretation of the core wrapper as the "isolation elements", in view of the claims rejected under 35 U.S.C. 112, first paragraph, as stated above, the Examiner broadly interprets the "isolation elements" to be equivalent to a core wrapper 24 positioned near each RAM 12 for isolating logic (14, 16) from the memory circuits (RAM) 12, where the wrapper includes scan chain bypass isolation elements (scan register 46) which enables and disables BIST 11, where the testing of the memory macro circuits (RAM) 12 is performed while the logic scan chain results are read out via a SCANOUT bus 23 to tester 21 by serially shifting the data outward from the logic circuits (14, 16).

Furthermore, the claimed invention does not recite the feature of, "the scan to occur simultaneously" as argued by the Applicant. In response to applicant's argument that the Kraus reference fails to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., "the scan to occur simultaneously")

are not recited in the rejected claims. Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JAMES C KERVEROS whose telephone number is (571) 272-3824. The examiner can normally be reached on 9:00 AM TO 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Examiner's Fax: (703) 746-4461
Email: james.kerveros@uspto.gov

Date: 18 January 2005
Office Action: Final Rejection

By: _____

JAMES C KERVEROS
Examiner
Art Unit 2133

Guy J. Lamarre
Primary Examiner